

## Claims

What is claimed is:

- 1           1.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2 apparatus comprising:  
3           a FIFO random access memory (RAM) having a data input for  
4 receiving data and control information and a data output for outputting said  
5 data and control information; said FIFO RAM including a plurality of locations  
6 for storing a plurality of words, each word including a set number of bits;  
7           write clocked logic for loading said data and control information to  
8 said FIFO RAM at a first clock frequency;  
9           asynchronous read clocked logic for outputting said data and control  
10 information from said FIFO RAM at a second clock frequency; and  
11           said first clock frequency of said write clocked logic and said second  
12 clock frequency of said asynchronous read clocked logic and a data width of  
13 said FIFO RAM being selectively provided for outputting said data and  
14 control information from said FIFO RAM with no back pressure.
- 1           2.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2 apparatus as recited in claim 1 wherein said FIFO RAM includes a multiple  
3 location FIFO RAM used on each asynchronous boundary.
- 1           3.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2 apparatus as recited in claim 1 wherein loading said data and control  
3 information enables predefined higher level functions including interleaving  
4 multiple direct memory accesses (DMAs), and providing an abort and  
5 discard data function.
- 1           4.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2 apparatus as recited in claim 1 wherein said data and control information  
3 includes a data field storing data being direct memory accessed (DMAed)  
4 through said FIFO RAM.

1           5.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing parity or error correction code (ECC) control  
4     information.

1           6.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing buffer address control information for writing a  
4     data field to a buffer of a target engine.

1           7.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing byte valid control information for writing a data  
4     byte from a data field to a buffer of a target engine.

1           8.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing engine select control information for selecting  
4     a target engine.

1           9.     A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing buffer select control information for selecting a  
4     buffer on a target engine.

1           10.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said data and control information  
3     includes a control field storing authorization code control information for  
4     discarding said data and control information being outputted from said FIFO  
5     RAM.

1           11.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2     apparatus as recited in claim 1 wherein said write clocked logic for loading  
3     said data and control information to said FIFO RAM at said first clock  
4     frequency includes a Gray code increment block encoding a write address  
5     input to said FIFO RAM.

1           12.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2    apparatus as recited in claim 11 includes a multiplexer coupled to said Gray  
3    code increment block and receiving a write strobe select input for  
4    incrementing a Gray code write address.

1           13.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2    apparatus as recited in claim 12 includes a pair of synchronization latches to  
3    provide a synchronization input to said asynchronous read clocked logic for  
4    outputting said data and control information from said FIFO RAM at said  
5    second clock frequency.

1           14.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2    apparatus as recited in claim 13 wherein said asynchronous read clocked  
3    logic for outputting said data and control information from said FIFO RAM at  
4    said second clock frequency includes a Gray code increment block encoding  
5    a read address input to said FIFO RAM.

1           15.    A flow through asynchronous elastic first-in, first-out (FIFO)  
2    apparatus as recited in claim 13 wherein said asynchronous read clocked  
3    logic includes a multiplexer coupled to said Gray code increment block  
4    encoding said read address input to said FIFO RAM and receiving a valid  
5    strobe select input for incrementing a Gray code read address.

1           16.    A method for implementing multi-engine parsing and  
2    authentication with a flow through asynchronous elastic first-in, first-out  
3    (FIFO) apparatus including a FIFO random access memory (RAM) having a  
4    data input for receiving data and a data output for outputting said data; the  
5    FIFO RAM including a plurality of locations for storing a plurality of words,  
6    each word including a set number of bits; said method comprising the steps  
7    of:

8           loading data and control information to the FIFO RAM at a first clock  
9    frequency;

10          outputting said data and control information from the FIFO RAM at a  
11    second clock frequency; and

12          selectively providing said first clock frequency and said second clock  
13    frequency and a data width of the FIFO RAM for outputting said data and  
14    control information from the FIFO RAM with no back pressure.

1           17.    A method as recited in claim 16 wherein the step of loading  
2   data and control information includes the steps of storing a data field and a  
3   plurality of control fields in the FIFO RAM.

1           18.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing an engine select control field  
3   for selecting a target engine.

1           19.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing an authorization code control  
3   field for discarding said data and control information being outputted from  
4   the FIFO RAM.

1           20.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing an address control field for  
3   writing a data field to a buffer of a target engine.

1           21.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing a byte valid control field for  
3   writing a data byte from a data field to a buffer of a target engine.

1           22.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing a buffer select control field for  
3   selecting a buffer of a target engine.

1           23.    A method as recited in claim 17 wherein the steps of storing  
2   said plurality of control fields including storing a parity or error correction  
3   code (ECC) control field for providing parity of ECC protection.